Claims

We claim:

1. A radio-frequency (RF) apparatus, comprising:

a first circuit partition comprising at least one of transmitter circuitry, receiver circuitry, or a combination thereof;

a second circuit partition coupled to said first circuit partition, said second circuit partition comprising baseband interface circuitry configured for coupling to baseband processor circuitry; and

a third circuit partition coupled to said second circuit partition and comprising frequency modification circuitry comprising at least one variable capacitance device, said frequency modification circuit being configured for coupling to a crystal to form a crystal oscillator circuit that is capable of providing an adjustable reference signal to said second circuit partition, and said at least one variable capacitance device being configured to adjust the frequency of said adjustable reference signal;

wherein said second circuit partition is configured to receive said adjustable reference signal and to provide said adjustable reference signal or a signal based on said adjustable reference signal to said first circuit partition.

2. The apparatus of claim 1, wherein said first circuit partition comprises a first integrated circuit that includes receiver analog circuitry and transmitter circuitry; wherein said second circuit partition comprises a second integrated circuit that includes receiver

digital circuitry; and wherein said third circuit partition comprises a third integrated circuit that includes said frequency modification circuitry and local oscillator circuitry.

3. The apparatus of claim 2, wherein said third circuit partition is configured for coupling to said baseband processor circuitry; and wherein said at least one variable capacitance device of said frequency modification circuitry is configured to adjust the frequency of said adjustable reference signal based at least in part on one or more frequency control signals received by said frequency modification circuitry, said one or more frequency control signals comprising signals provided by said baseband processor circuitry or comprising signals that are based on signals provided by said baseband processor circuitry.

4. The apparatus of claim 3, wherein said second circuit partition is configured to provide an adjustable reference signal or a signal based on said adjustable reference signal to said baseband processor circuitry.

5. The apparatus of claim 4, wherein said second circuit partition further comprises reference clock buffer circuitry configured to receive said adjustable reference signal from said third circuit partition and to provide a buffered reference clock signal based on said adjustable reference signal to said first circuit partition and to said baseband processor circuitry.

6. The apparatus of claim 3, wherein said at least one variable capacitance device comprises at least one continuously variable capacitor, at least one discretely variable capacitor, or a combination thereof.

7. The apparatus of claim 3, wherein said frequency modification circuitry comprises at least one continuously variable capacitor and at least one discretely variable capacitor, each of said at least one continuously variable capacitor and said at least one discretely variable capacitor being configured to adjust the frequency of said adjustable

reference signal in response to said one or more frequency control signals received by said frequency modification circuitry.

8. The apparatus of claim 3, wherein said variable capacitance device comprises:

variable capacitor circuitry configured to adjust the frequency of said adjustable reference signal in response to a plurality of control voltage signals; and

control circuitry, the control circuitry configured to generate the plurality of control voltage signals in response to at least one of said one or more frequency control signals;

wherein the voltage level of each of the plurality of the control voltage signals differs by an offset voltage from the voltage level of the remaining signals in the plurality of control voltage signals.

9. The apparatus of claim 3, wherein said variable capacitance device comprises a digitally programmable capacitor array configured to adjust the frequency of said adjustable reference signal in response to a plurality of frequency control signals generated by a digitally programmable capacitor array register.

10. The apparatus of claim 3, wherein said one or more frequency control signals comprise analog signals provided by said baseband processor circuitry, or comprise signals based on analog signals provided by said baseband processor circuitry.

11. A radio-frequency (RF) apparatus, comprising:

a first circuit partition comprising at least one of transmitter circuitry, receiver circuitry, or a combination thereof;

a second circuit partition coupled to said first circuit partition, said second circuit partition comprising baseband interface circuitry configured for coupling to baseband processor circuitry; and

a third circuit partition coupled to said second circuit partition and comprising:

frequency modification circuitry comprising at least one variable capacitance device, said frequency modification circuit being configured for coupling to a crystal to form a crystal oscillator circuit that is capable of providing an adjustable reference signal to said second circuit partition, and said at least one variable capacitance device being configured to adjust the frequency of said adjustable reference signal based at least in part on one or more analog frequency control signals received by said frequency modification circuitry, and

digital-to-analog conversion (DAC) circuitry coupled to said frequency modification circuit, said DAC circuitry being configured to receive one or more digital frequency control signals and to generate and provide at least a portion of said one or more analog frequency control signals to said frequency modification circuit based on said one or more digital frequency control signals;

wherein said second circuit partition is configured to receive said adjustable reference signal and to provide said adjustable reference signal or a signal based on said adjustable reference signal to said first circuit partition.

12. The apparatus of claim 11, wherein said first circuit partition comprises a first integrated circuit that includes receiver analog circuitry and transmitter circuitry; wherein said second circuit partition comprises a second integrated circuit that includes receiver digital circuitry; and wherein said third circuit partition comprises a third integrated

circuit that includes said frequency modification circuitry, said DAC circuitry, and local oscillator circuitry.

13. The apparatus of claim 12, wherein said third circuit partition is configured for coupling to said baseband processor circuitry; and wherein said one or more digital frequency control signals comprise signals provided by said baseband processor circuitry or comprise signals that are based on signals provided by said baseband processor circuitry.

14. The apparatus of claim 13, wherein said second circuit partition is configured to provide an adjustable reference signal or a signal based on said adjustable reference signal to said baseband processor circuitry.

15. The apparatus of claim 14, wherein said second circuit partition further comprises reference clock buffer circuitry configured to receive said adjustable reference signal from said third circuit partition and to provide a buffered reference clock signal based on said adjustable reference signal to said first circuit partition and to said baseband processor circuitry.

16. The apparatus of claim 13, wherein said at least one variable capacitance device comprises at least one continuously variable capacitor.

17. The apparatus of claim 13, wherein said frequency modification circuitry comprises at least one continuously variable capacitor and at least one discretely variable capacitor, each of said at least one continuously variable capacitor and said at least one discretely variable capacitor being configured to adjust the frequency of said adjustable reference signal in response to one or more frequency control signals, said at least one continuously variable capacitor being configured to adjust the frequency of said adjustable reference signal in response to said one or more analog frequency control signals received by said frequency modification circuitry from said DAC circuitry.

18. The apparatus of claim 13, wherein said variable capacitance device comprises:

variable capacitor circuitry configured to adjust the frequency of said adjustable reference signal in response to a plurality of control voltage signals; and

control circuitry, the control circuitry configured to generate the plurality of control voltage signals in response to at least one of said one or more analog frequency control signals received by said frequency modification circuitry from said DAC circuitry;

wherein the voltage level of each of the plurality of the control voltage signals differs by an offset voltage from the voltage level of the remaining signals in the plurality of control voltage signals.

19. The apparatus of claim 18, wherein said frequency modification circuitry further comprises a digitally programmable capacitor array configured to adjust the frequency of said adjustable reference signal in response to a plurality of frequency control signals generated by a digitally programmable capacitor array register.

20. The apparatus of claim 13, wherein said one or more digital frequency control signals comprise signals generated by automatic frequency control (AFC) control circuitry within said baseband processor circuitry.

21. A radio-frequency (RF) apparatus, comprising:

a first circuit partition comprising at least one of transmitter circuitry, receiver circuitry, or a combination thereof; and

a second circuit partition coupled to said first circuit partition and configured for coupling to baseband processor circuitry, said second circuit partition

comprising frequency modification circuitry comprising at least one variable capacitance device, said frequency modification circuit being configured for coupling to a crystal to form a crystal oscillator circuit that is capable of providing an adjustable reference signal or a signal based on said adjustable reference signal to said first circuit partition, and said at least one variable capacitance device being configured to adjust the frequency of said adjustable reference signal.

22. The apparatus of claim 21, wherein said first circuit partition comprises a first integrated circuit that includes receiver analog circuitry and transmitter circuitry; and wherein said second circuit partition comprises a third integrated circuit that includes said frequency modification circuitry and local oscillator circuitry.

23. The apparatus of claim 22, wherein said second circuit partition is configured for coupling to baseband processor circuitry that comprises receiver digital circuitry.

24. The apparatus of claim 23, wherein said at least one variable capacitance device of said frequency modification circuitry is configured to adjust the frequency of said adjustable reference signal based at least in part on one or more frequency control signals received by said frequency modification circuitry, said one or more frequency control signals comprising signals provided by said baseband processor circuitry or comprising signals that are based on signals provided by said baseband processor circuitry.

25. The apparatus of claim 24, wherein said second circuit partition is configured to provide an adjustable reference signal or a signal based on said adjustable reference signal to said baseband processor circuitry.

26. The apparatus of claim 25, wherein said second circuit partition further comprises reference clock buffer circuitry configured to receive said adjustable reference signal from said frequency modification circuitry and to provide a buffered reference clock

signal based on said adjustable reference signal to said first circuit partition and to said baseband processor circuitry.

27. The apparatus of claim 24, wherein said at least one variable capacitance device comprises at least one continuously variable capacitor, at least one discretely variable capacitor, or a combination thereof.

28. The apparatus of claim 24, wherein said frequency modification circuitry comprises at least one continuously variable capacitor and at least one discretely variable capacitor, each of said at least one continuously variable capacitor and said at least one discretely variable capacitor being configured to adjust the frequency of said adjustable reference signal in response to said one or more frequency control signals received by said frequency modification circuitry.

29. The apparatus of claim 24, wherein said variable capacitance device comprises:

variable capacitor circuitry configured to adjust the frequency of said adjustable reference signal in response to a plurality of control voltage signals; and

control circuitry, the control circuitry configured to generate the plurality of control voltage signals in response to at least one of said one or more frequency control signals;

wherein the voltage level of each of the plurality of the control voltage signals differs by an offset voltage from the voltage level of the remaining signals in the plurality of control voltage signals.

30. The apparatus of claim 24, wherein said variable capacitance device comprises a digitally programmable capacitor array configured to adjust the frequency of said adjustable reference signal in response to a plurality of frequency control signals generated by a digitally programmable capacitor array register.

31. The apparatus of claim 24, wherein said one or more frequency control signals comprise analog signals provided by said baseband processor circuitry, or comprise signals based on analog signals provided by said baseband processor circuitry.

32. A radio-frequency (RF) apparatus comprising a first circuit partition, said first circuit partition comprising:

at least one of transmitter circuitry, receiver circuitry, or a combination thereof;

frequency modification circuitry coupled to said transmitter circuitry, receiver circuitry, or a combination thereof, said frequency modification circuitry comprising at least one variable capacitance device, said frequency modification circuit being configured for coupling to a crystal to form a crystal oscillator circuit that is capable of generating an adjustable reference signal and of providing said adjustable reference signal to said transmitter circuitry, receiver circuitry, or a combination thereof, said at least one variable capacitance device configured to adjust the frequency of said adjustable reference signal based at least in part on one or more analog frequency control signals received by said frequency modification circuitry; and

wherein said first circuit partition is configured for coupling to baseband processor circuitry.

33. The apparatus of claim 32, wherein said first circuit partition is integrated within a single integrated circuit.

34. The apparatus of claim 32, wherein said first circuit partition further comprises local oscillator circuitry coupled to said transmitter circuitry, receiver circuitry, or a combination thereof; and digital-to-analog conversion (DAC) circuitry coupled to said

frequency modification circuitry, said DAC circuitry being configured to receive one or more digital frequency control signals and to generate and provide at least a portion of said one or more analog frequency control signals to said frequency modification circuit based on said one or more digital frequency control signals.

35. The apparatus of claim 34, wherein said first circuit partition comprises transceiver circuitry that includes receiver analog circuitry and transmitter circuitry; and receiver digital circuitry coupled to said transceiver circuitry; wherein said local oscillator circuitry is coupled to said transceiver circuitry.

36. The apparatus of claim 35, wherein said first circuit partition is integrated within a single integrated circuit.

37. The apparatus of claim 36, wherein said receiver digital circuitry and said DAC circuitry are each configured for coupling to said baseband processor; and wherein said one or more digital frequency control signals comprise signals provided by said baseband processor circuitry or comprise signals that are based on signals provided by said baseband processor circuitry.

38. The apparatus of claim 37, wherein said first circuit partition is configured to provide an adjustable reference signal or a signal based on said adjustable reference signal to said baseband processor circuitry.

39. The apparatus of claim 38, wherein said first circuit partition further comprises reference clock buffer circuitry configured for coupling to said baseband processor circuitry, said reference clock buffer circuitry configured to receive said adjustable reference signal from said crystal oscillator circuit and to provide a buffered reference clock signal based on said adjustable reference signal to said baseband processor circuitry.

40. The apparatus of claim 37, wherein said at least one variable capacitance device comprises at least one continuously variable capacitor.

41. The apparatus of claim 37, wherein said frequency modification circuitry comprises at least one continuously variable capacitor and at least one discretely variable capacitor, each of said at least one continuously variable capacitor and said at least one discretely variable capacitor being configured to adjust the frequency of said adjustable reference signal in response to one or more frequency control signals, said at least one continuously variable capacitor being configured to adjust the frequency of said adjustable reference signal in response to said one or more analog frequency control signals received by said frequency modification circuitry from said DAC circuitry.

42. The apparatus of claim 37, wherein said variable capacitance device comprises:

variable capacitor circuitry configured to adjust the frequency of said adjustable reference signal in response to a plurality of control voltage signals; and

control circuitry, the control circuitry configured to generate the plurality of control voltage signals in response to at least one of said one or more analog frequency control signals received by said frequency modification circuitry from said DAC circuitry;

wherein the voltage level of each of the plurality of the control voltage signals differs by an offset voltage from the voltage level of the remaining signals in the plurality of control voltage signals.

43. The apparatus of claim 42, wherein said frequency modification circuitry further comprises a digitally programmable capacitor array configured to adjust the frequency of said adjustable reference signal in response to a plurality of frequency control signals generated by a digitally programmable capacitor array register.

44. The apparatus of claim 37, wherein said one or more digital frequency control signals comprise signals generated by automatic frequency control (AFC) control circuitry within said baseband processor circuitry.

45. The apparatus of claim 36, wherein said first circuit partition further comprises AFC control circuitry, said AFC circuitry being configured to provide at least a portion of said analog frequency control signals.

46. The apparatus of claim 45, wherein said AFC control circuitry is configured to generate one or more of said analog frequency control signals based at least in part on a signal representative of temperature, a baseband frequency control signal received from said baseband processor circuitry, or a combination thereof.